REMARKS

Prior to the present response, claims 1, 3-7, 9-16, and 18-20 were pending in the present application, and remain pending in the present application. Reconsideration and allowance of pending claims 1, 3-7, 9-16, and 18-20 in view of the following remarks are respectfully requested.

In the Office Action dated November 1, 2005, the Examiner has ***finally rejected*** outstanding claims 1, 3-7, 9-16, and 18-20 in the present application on the basis of new ground(s) of rejection and newly cited art. Applicants respectfully request reconsideration and withdrawal of the finality of the rejection in the Office Action dated November 1, 2005.

A good and sufficient reason why the present response is necessary and was not earlier presented is that an entirely new reference has been cited in the present final rejection dated November 1, 2005 (37 CFR §1.116(c)). The new reference is U.S. Patent Number 6,521,997 to Huang et al. (hereinafter "Huang"), which is for the first time brought to Applicants' attention by means of the present ***final rejection*** dated November 1, 2005. The new reference, i.e. Huang, was not cited in the present application prior to the instant final rejection. Since Huang is a reference upon which the Examiner has now relied, Applicants believe that it would be manifestly unfair for the Patent Office not to consider Applicants' arguments, which are necessitated due to the newly cited reference, Huang.

A. **Rejections of Claims 1, 3-7, 9-16, and 18-20 under 35 USC §103(a)**

The Examiner has rejected claims 1, 3-7, 9-16, and 18-20 under 35 USC §103(a) as being unpatentable over U.S. Patent Number 5,969,461 to Anderson et al. (hereinafter, "Anderson") in view of U.S. Patent Number 5,720,100 to Skipor et al. (hereinafter, "Skipor") and further in view of Huang. For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1, 9, and 16, is patentably distinguishable over Anderson, Skipor and Huang, either singly or in combination.

The present invention, as defined by independent claims 1, 9 and 16, includes a surface mount component (also referred to as "SMC"), having first and second terminals, where the SMC and its terminals are situated over a *laminate circuit board* (e.g., laminate circuit board 104 in Figure 1 or laminate circuit board 304 in Figure 3). First and second pads are also situated on the laminate circuit board and are coupled to the first and second terminals, respectively. As part of the solution to the shortcomings of the conventional technology, solder mask trench 124 (seen in Figure 1) is formed under a SMC, such as SMC 102 or SMC 302. More importantly, solder mask trench 124 is formed where, in the absence of the present invention, no solder mask opening or trench would be formed. In other words, except for and in the absence of the solder mask trench, the top surface of the laminate circuit board would be uniformly covered with solder mask.

Referring to Figure 1, by forming solder mask trench 124 (in an otherwise uniform blanket of solder mask) underneath the SMC and within solder mask 112, moldable gap 125, with an increased height 128, is advantageously formed and is substantially larger than a conventional moldable gap. By contrast, in a conventional structure, solder mask 112 would fill the region between pads 106 and 108 underneath the SMC. As a result, a conventional moldable gap that would be formed between solder mask 112 and the bottom surface of the SMC would have a reduced height 130, as shown in Figure 1 of the present application.

Thus, by etching solder mask trench 124 within a uniform blanket of solder mask 112, embodiments according to the present invention advantageously achieve a significantly larger moldable gap, having height 128, that improves molding compound flow underneath the SMC and, consequently, minimizes void formation underneath the SMC. As a result, embodiments according to the present invention advantageously minimize the risk of shorting between the terminals of the SMC during, for example, reflow assembly. See, for example, the present application page 9, lines 19-21. Indeed, since the invention does not require complex changes to the existing technology, the disadvantages of the existing technology in having voids in molding compounds under an SMC are overcome without significantly increasing manufacturing costs. Thus, among other advantages, the reliability of the SMC and the overmolded MCM itself can be significantly increased in an economic manner.

In contrast to the present invention, the disclosure in Anderson is directed to providing a package that encapsulates a "surface acoustic wave (SAW) device" such that the active area of the SAW device is isolated within a periphery of the device to prevent contamination. See, for example, column 2, lines 12-13 and 23-24. As acknowledged by the Examiner, Anderson does not disclose filling a solder mask trench with molding compound. In fact, Anderson teaches away from the present invention by effectively preventing the flow of any molding compound by disposing dam 26 on top 30 of substrate 16 between substrate 16 and acoustic wave device 10. See, for example, Anderson, column 3, lines 29-31 and 48-56.

For example, Anderson teaches the use of a dam that is "a photolithographically-defined standard solder mask material" which "prevents intrusion of foreign materials during overmolding and at any other time." See Anderson, column 3, lines 39-40 and lines 54-56. Thus, Anderson teaches away from forming a solder mask trench underneath acoustic wave device 10 to facilitate the flow of molding compound because the disclosure in Anderson prevents the flow of molding compound (underfill material 28) by using dam 26 (albeit that dam 26 is comprised of solder mask) to provide a sealed cavity 34 (i.e. a cavity void of molding compound). See, for example, Figure 2 of Anderson and column 5, lines 10-15.

Skipor, in contrast to the present invention, discloses an "assembly in which an integrated circuit die is spaced apart from a printed circuit board by a gap and is attached by solder bump interconnections that extend across the gap and connect bond pads on the

die to bond pads on the board." Skipor, column 1, lines 59-63. More specifically, Figure 2 reveals that gap 30 is defined by die bond pads 28, solder bump interconnections 32, and board bond pads 22. As such, the gap in Skipor does not equate to a solder mask trench as required by the present invention. Moreover, Skipor does not make any reference to, nor even mentions, the phrase "solder mask" anywhere in its disclosure. Skipor merely discloses a structure spaced apart by a gap that occurs as a result of the particular assembly involved and not by modifying the solder mask as required by the present invention.

In contrast to the present invention, Huang discloses a chip carrier technology that includes a *core layer* defined with a chip attach area. See, for example, Huang, column 3, lines 5-8. Thus, the disclosure in Huang does not teach, disclose, or suggest the use of a *laminate circuit board* as disclosed and claimed by the present invention. Moreover, Huang actually teaches away from the use of a laminate circuit board by disclosing that: "chip carrier 1' [sic] of the second embodiment [shown in Figure 4 of Huang] is structurally identical to that of the first embodiment [shown in Figures 1 and 2 of Huang], as both are a substrate for use in a BGA (ball grid array) semiconductor package." Huang, column 4, lines 5-8. Thus, Huang is directed to a discrete chip packaging technology and not to a laminate printed circuit board as disclosed and claimed by the present invention. In other words, Huang's ball grid array semiconductor package is mounted onto a laminate printed circuit board, such as that disclosed and claimed by the present invention. Thus, Huang is directed to a discrete semiconductor packaging

technology, while the present invention is directed to a laminate printed circuit board technology, the latter being suitable for hosting a discrete semiconductor package, such as Huang's semiconductor package. Huang, therefore, is directed to a different technology (i.e., to BGA semiconductor packaging) than the present invention. As such, Huang does not teach, disclose, or suggest a solder mask trench that *"is situated over a top surface of said laminate circuit board,"* as recited by independent claims 1, 9, and 16 of the present invention.

Huang also fails to teach, disclose, or suggest a solder mask that "uniformly covers said top surface of said laminate circuit board," as recited by independent claims 1, 9, and 16 of the present invention. The disclosure in Huang merely explains that: "trace forming area 101 is applied with a solder mask layer 11 for covering the conductive traces on the trace forming area 101." Huang, column 3, lines 12-14. Moreover, Figures 1 through 4 in Huang only show a portion of the solder mask layer and thus do not show a solder mask that uniformly covers the entire core layer. Thus, Huang does not suggest a solder mask layer which uniformly covers the core layer. In fact, Huang actually limits the coverage of the solder mask by disclosing that only trace forming area 101 is subject to application of solder mask layer 11.

In further contrast to the present invention, Huang also does not teach, disclose, or suggest a solder mask *trench* situated over a top surface of a laminate circuit board, as required by the present invention. Huang discloses that: "a *recessed portion* 13 is formed at the solder mask layer 11 between the pair of solder pads 12." Huang, column 3, lines

20-22 (emphasis added). Referring to the elliptical "recess" shown in Figure 1, this recess in Huang does not suggest the use of a solder mask trench as required by the present invention.

Thus, Huang does not teach, disclose, or suggest a solder mask trench that is situated over a top surface of a laminate circuit board, "wherein a solder mask uniformly covers said top surface of said laminate circuit board," as recited by independent claims 1, 9, and 16 of the present invention. Furthermore, since Huang is directed to a different technology than the present invention, the present invention cannot be achieved by combining Huang with the disclosures in Anderson and Skipor.

Applicants, therefore, respectfully submit that the disclosures in Anderson, Skipor, and Huang contain no motivation or suggestion to combine the cited references. Anderson discloses a package that encapsulates a SAW device where the active area of the SAW device is isolated within a periphery of the device to prevent contamination, thus effectively *preventing* the flow of molding compound underneath the SAW device. Skipor, on the other hand, discloses a microelectronic assembly that includes an integrated circuit die spaced apart from a printed circuit board by a gap, which is then underfilled with a molding compound, but without any suggestions of modifying a solder mask layer or even mentioning the phrase "solder mask" anywhere in the disclosure. As such, the disclosures in Anderson and Skipor are fundamentally different and cannot be combined with Huang to achieve the present invention.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by independent claims 1, 9, and 16 is not taught, disclosed, or suggested by the art of record. As such, the claims depending from independent claims 1, 9, and 16 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 9, and 16, and the claims depending therefrom, is patentably distinguishable over the cited art. Thus, outstanding claims 1, 3-7, 9-16, and 18-20 are patentably distinguishable over the cited art. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1, 3-7, 9-16 and 18-20 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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